Fig. 1

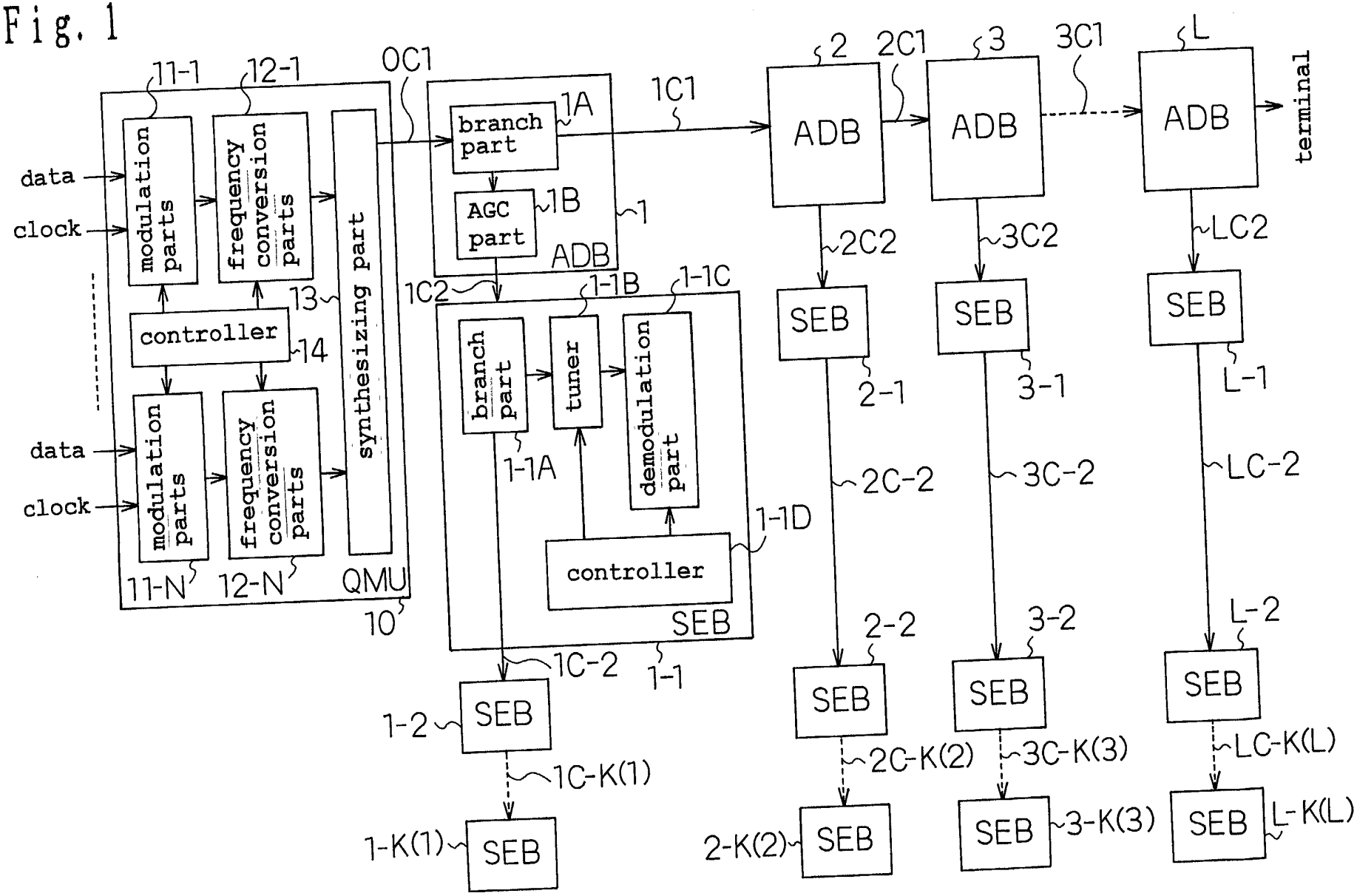

11-1
12-1
0C1
data
clock
modulation parts
frequency conversion parts
synthesizing part
controller
13
14
data
clock
modulation parts
frequency conversion parts
11-N
12-N
QMU
10
branch part
1A
AGC part
1B
ADB
1
1C1
1C2
1-1B
1-1C
branch part
tuner
demodulation part
1-1A
controller
1-1D
SEB
1-1
1C-2
1-2
SEB
1C-K(1)
1-K(1)
SEB
2
2C1
3
3C1
L
ADB
ADB
ADB
terminal
2C2
3C2
LC2
SEB
SEB
SEB
2-1
3-1
L-1
2C-2
3C-2
LC-2
2-2
3-2
L-2
SEB
SEB
SEB
2C-K(2)
3C-K(3)
LC-K(L)
2-K(2)
SEB
SEB
3-K(3)
SEB
L-K(L)

Fig. 2

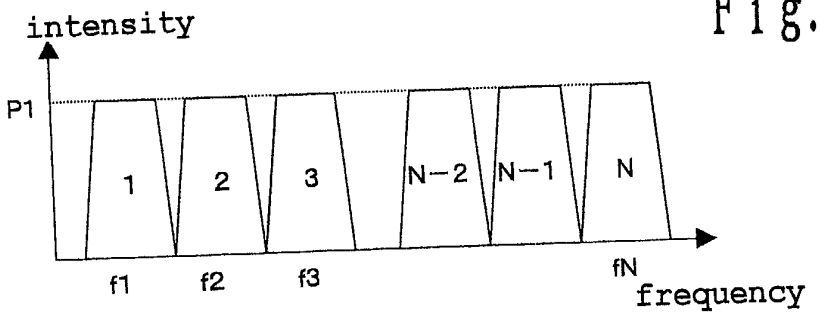


Fig. 5

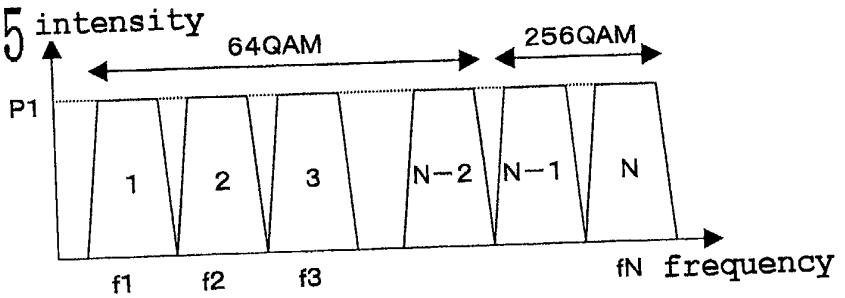


Fig. 3

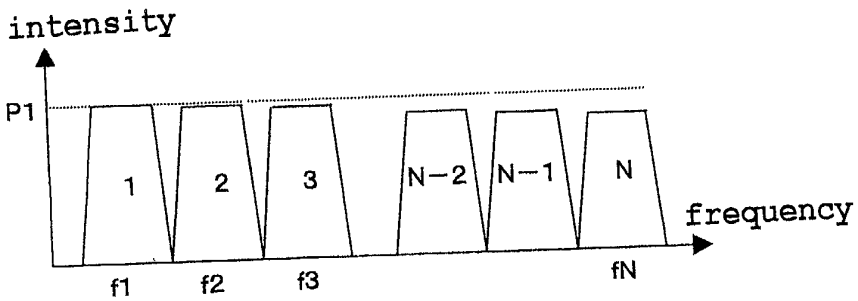


Fig. 4

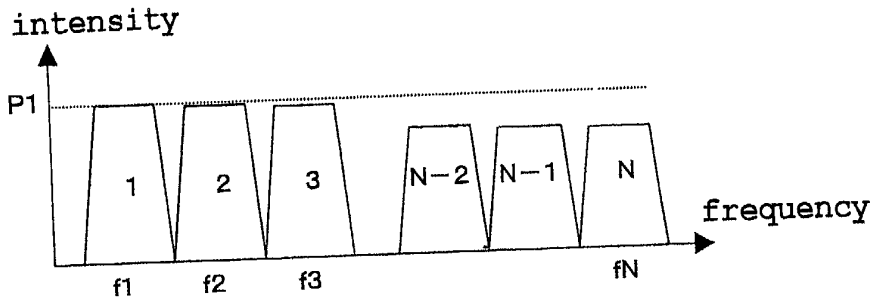
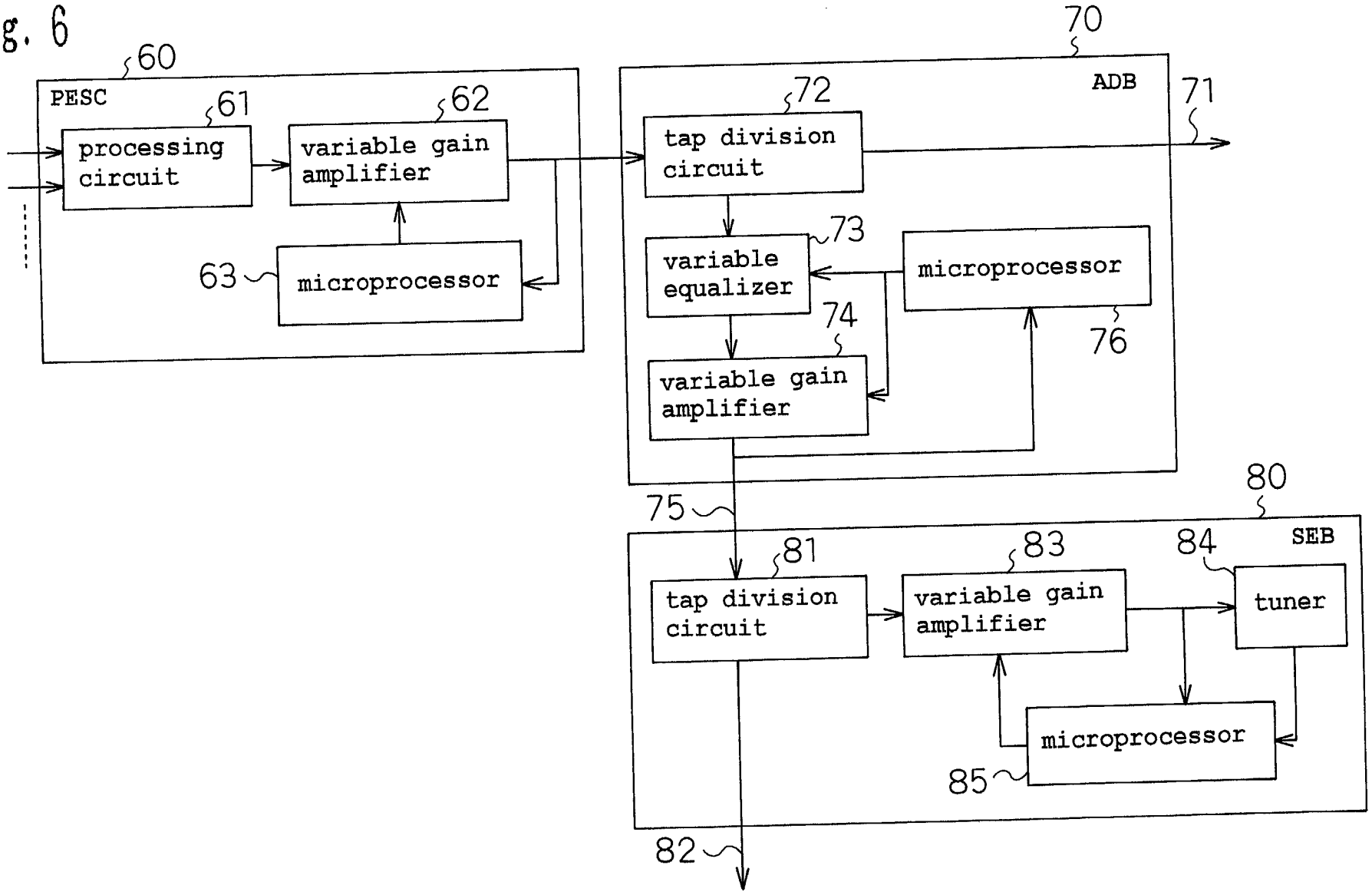


Fig. 6


60
PESC
61
processing circuit
62
variable gain amplifier
63
microprocessor
70
ADB
71
72
tap division circuit
73
variable equalizer
microprocessor
74
variable gain amplifier
76
75
80
SEB
81
tap division circuit
83
variable gain amplifier
84
tuner
microprocessor
85
82